



512 x 512 pixel format
(24 μ m square)



Front-illuminated or thinned,
back-illuminated versions



Unique thinning and Quantum
Efficiency enhancement processes



Excellent QE from IR to UV



Anti-reflection coating
for visible region



Mechanical Rigidity



MPP technology



Low dark current



Excellent charge transfer efficiency
(CTE) at all signal levels



On-chip output MOSFET
for low noise



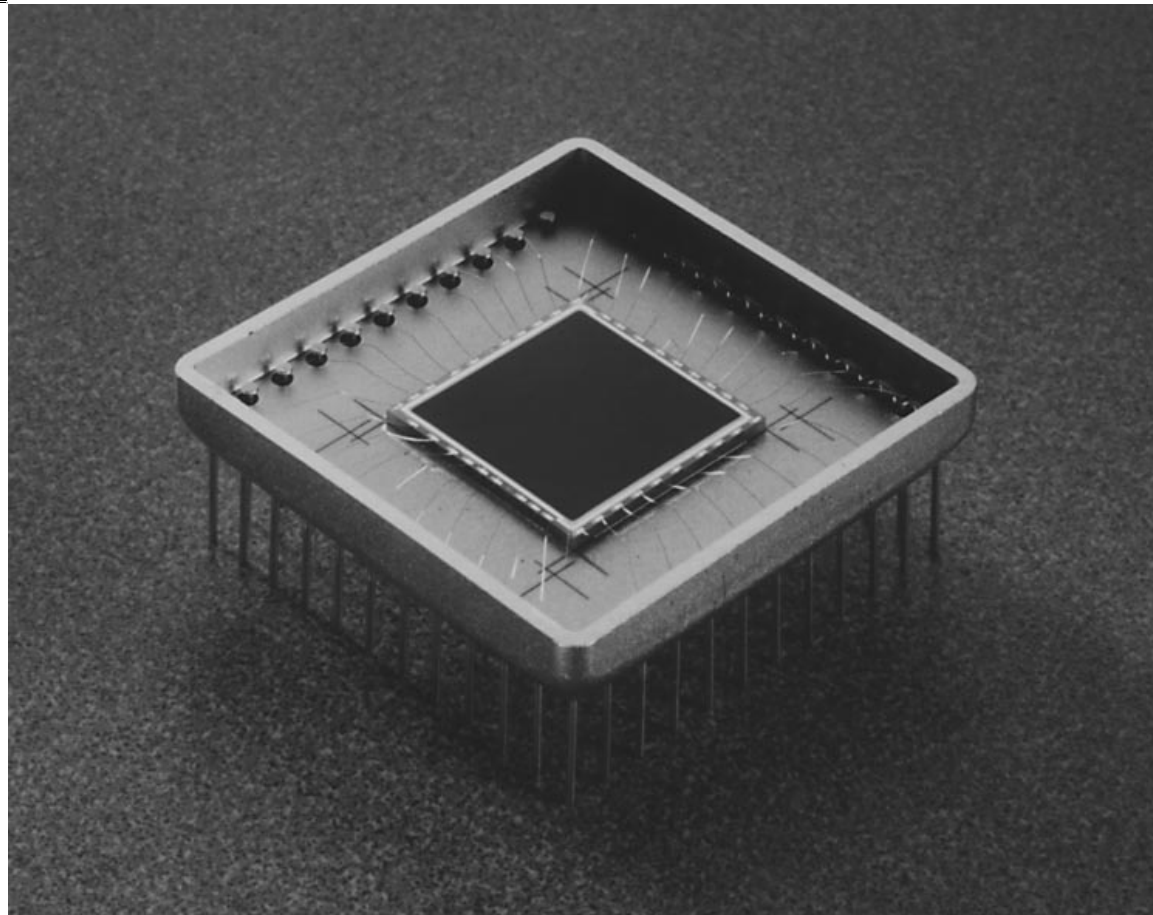
Wide dynamic range



Selectable bi-directional read-out
of imaging data



Applications include astronomy,
machine vision, medical imaging,
and scientific imaging



SITe 512 x 512 Scientific-Grade CCD

SI-502A CCD Imager: *Ideal for applications with small-area imaging requirements*

General Description

The SI-502A CCD Imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from UV to near infrared. The sensor is fabricated as a 512 x 512 pixel, full frame area imager that utilizes a buried channel, three level polysilicon gate process. Features include a buried channel with a mini-channel for high transfer efficiency, multi-phase pinned (MPP) operation for low dark current, and lightly doped drain (LDD) output amplifier for low read noise. The device is available in a front

illuminated version or a thinned, back-illuminated version that provides superior quantum efficiency.

SITe's unique thinning and back surface enhancement process provides increased blue and UV response in a flat and fully supported die. It is more rugged and easier to uniformly cool than fragile edge-supported chips. The CCD imager is mounted in a non-hermetic metal package without a window.

advantages of MPP operation are the reduction of the surface residual image defect and a greater tolerance for ionizing radiation environments.

To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to the substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface, minimizing surface dark current

generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phases 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity

is about 50 percent of that of a standard CCD if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

DEVICE SPECIFICATIONS

Measured at -45 deg. C, unless otherwise indicated, 45 kpixels/sec and standard voltages using a dual slope CDS circuit (8 μ s integration time)

	Minimum	Typical	Maximum
Format		512 x 512 pixels	
Pixel Size		24 μ m x 24 μ m	
Imaging Area		12.3 mm x 12.3 mm	
Dark current (MPP), 20°C equivalent		50 pa/cm ²	70 pa/cm ²
Readout noise	Front	5 electrons	7 electrons
	Back	7 electrons	9 electrons
Full Well signal	300,000 electrons	350,000 electrons	
Output gain	1.0 μ V/ electron	1.5 μ V/ electron	
CTE per pixel	0.99995	0.99999	

TABLE 1 Device specifications, SI-502A

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	STANDARD	MAX	UNIT
VDDx	OUTPUT DRAIN SUPPLY	22	24	26	V
RDx	RESET DRAIN	13	15	17	V
LGx	LAST GATE	-4	-2	0	V
SUB,PKG	SUB & PACKAGE CONNECTION		0		V
ID	INPUT DIODE SUPPLY	5	15	26	V
GNDx	MOSFET GROUND REFERENCE		0		V
OUTx	MOSFET OUTPUT (LOAD)	5	20	50	kohms

GATE TO SUBSTRATE VOLTAGES

TERMINAL	ITEM	MIN	STANDARD	MAX	P TO P MAX	UNIT	
RGx	RESET GATE	LOW RAIL	-5	0	5	20	V
		HIGH RAIL	5	12	15		V
S#x	SERIAL GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
SWx	SUMMING WELL	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
P#x	PARALLEL GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	4	10		V
P3		HIGH RAIL	0	7	10		V
TGx	TRANSFER GATE	LOW RAIL	-10	-9	0	15	V
		HIGH RAIL	0	7	10		V
SG	SAMPLE GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V

TABLE 2 DC operating conditions and clock voltages, SI-502A

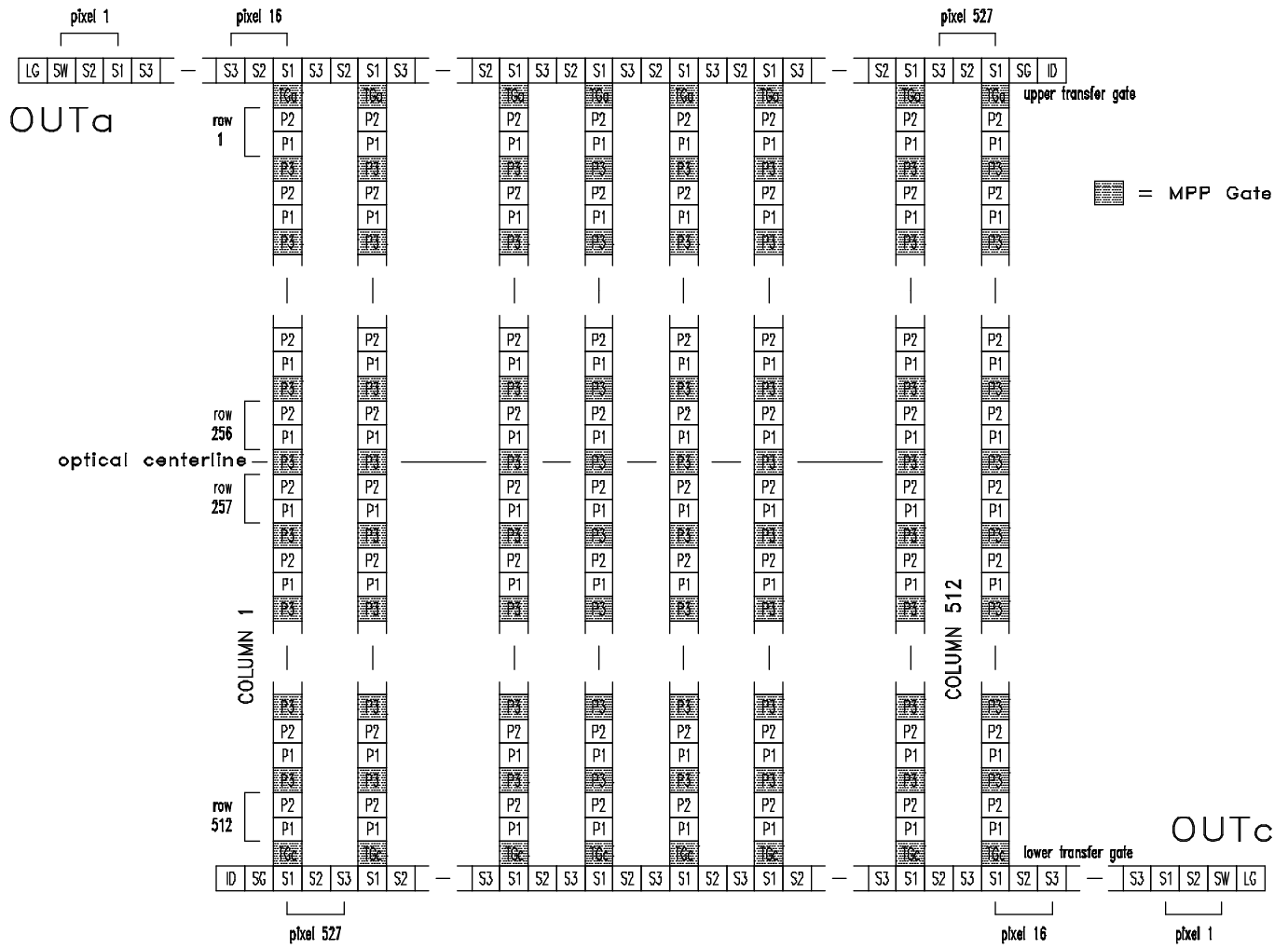
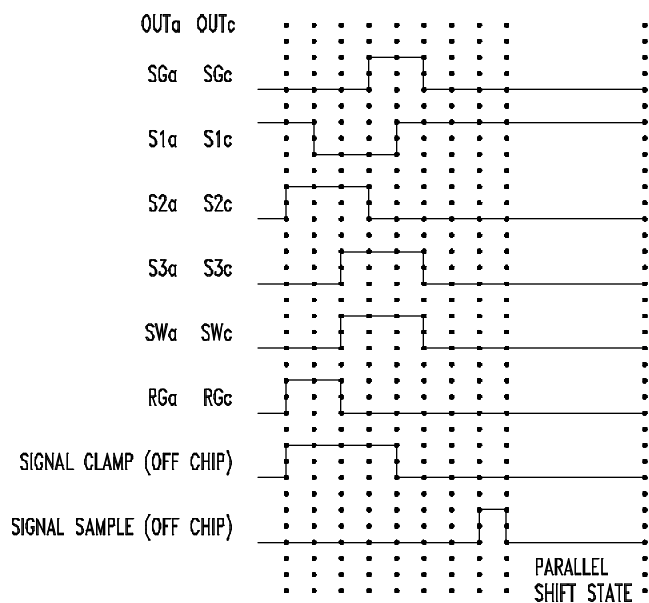
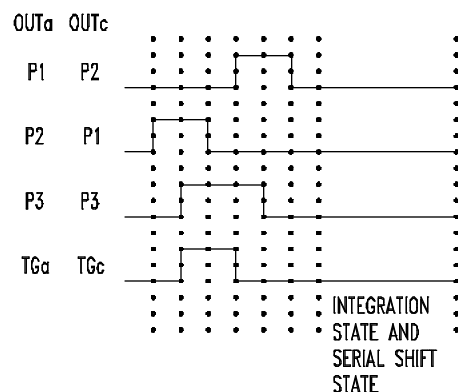


FIGURE 2 SI-502A functional diagram



SERIAL SHIFT TIMING



MPP PARALLEL SHIFT TIMING

FIGURE 3 SI-502A Serial and Parallel timing for both A and C outputs

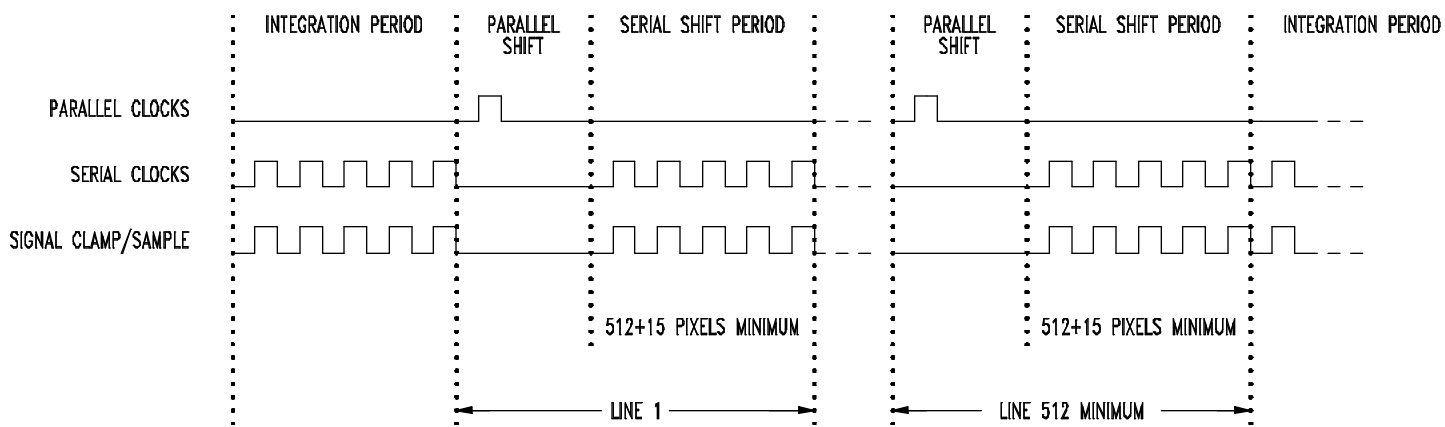


FIGURE 4 SI-502A Typical full-frame readout

SI-502A PIN DEFINITION

FRONT PIN #	BACK PIN #	FUNCTION	REGISTERS	SYMBOL
1	12	Substrate and Package Ground		SUB
2	11	Output transistor source, a output	a register	OUTa
3	10	Output Ground Reference	a register	GNDa
4	9	Transfer gate, upper serial register	a register	TGa
5	8	Parallel phase 3	image area	P3
6	7	Parallel phase 1	image area	P1
7	6	Parallel phase 2	image area	P2
8	5	Transfer gate, lower serial register	c register	TGc
9	4	Input diode	c register	IDc
10	3	input sample gate	c register	SGc
11	2	Serial phase 1, c register	c register	S1c
12	1	Substrate and Package Ground		SUB
13	44			N/C
14	43	Serial phase 2, c register	c register	S2c
15	42	*Temp. sense resistor		TR1
16	41	*Temp. sense resistor		TR2
17	40	Serial phase 3, c register	c register	S3c
18	39	Summing well, c output	c register	SWc
19	38	Last gate, c output	c register	LGc
20	37	Reset Gate, c output	c register	RGc
21	36	Reset Drain Supply, c output	c register	RDc
22	35			N/C
23	34			N/C
24	33	Output transistor drain, c output	c register	VDDc
25	32	Output transistor source, c output	c register	OUTc
26	31	Output Ground Reference	c register	GNDc
27	30	Transfer gate, lower serial register	c register	TGc
28	29	Parallel phase 3	image area	P3
29	28	Parallel phase 1	image area	P1
30	27	Parallel phase 2	image area	P2
31	26	Transfer gate, upper serial register	a register	TGa
32	25	Input diode	a register	IDa
33	24	input sample gate	a register	SGa
34	23			N/C
35	22			N/C
36	21	Serial phase 3, a register	a register	S3a
37	20	Serial phase 2, a register	a register	S2a
38	19	Serial phase 1, a register	a register	S1a
39	18	Summing well, a output	a register	SWa
40	17	Last gate, a output	a register	LGa
41	16	Reset transistor gate, a output	a register	RGa
42	15	Reset transistor drain, a output	a register	RDa
43	14	Output transistor drain, a output	a register	VDDa
44	13			N/C

TABLE 3 SI-502A pin definitions

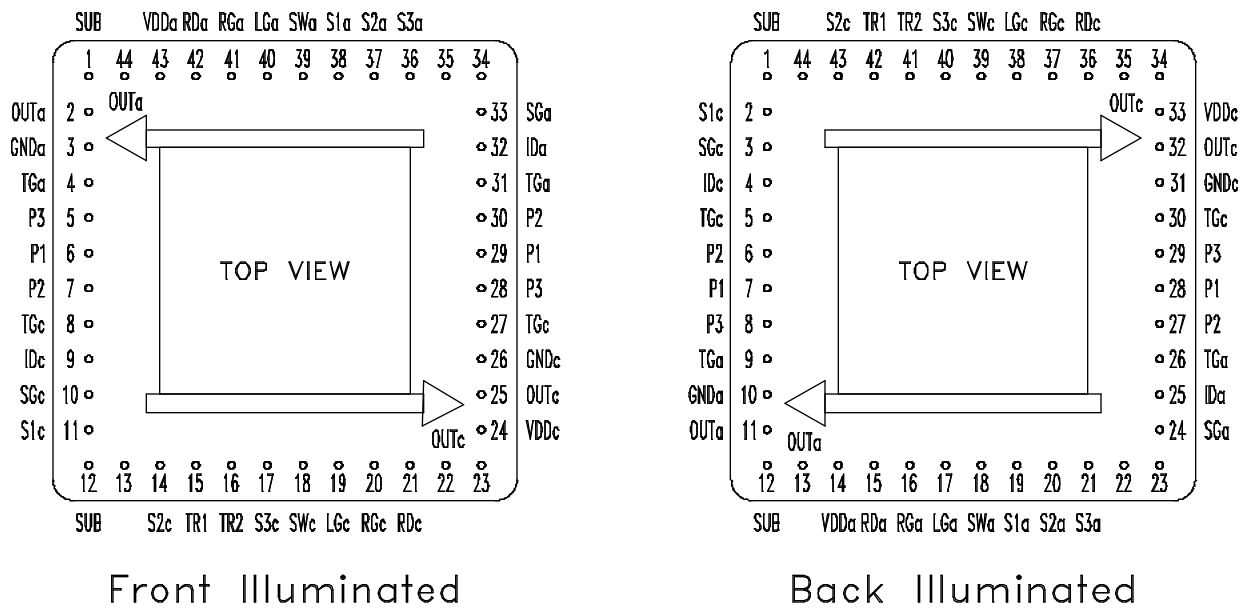


FIGURE 5 SI-502A pin labels

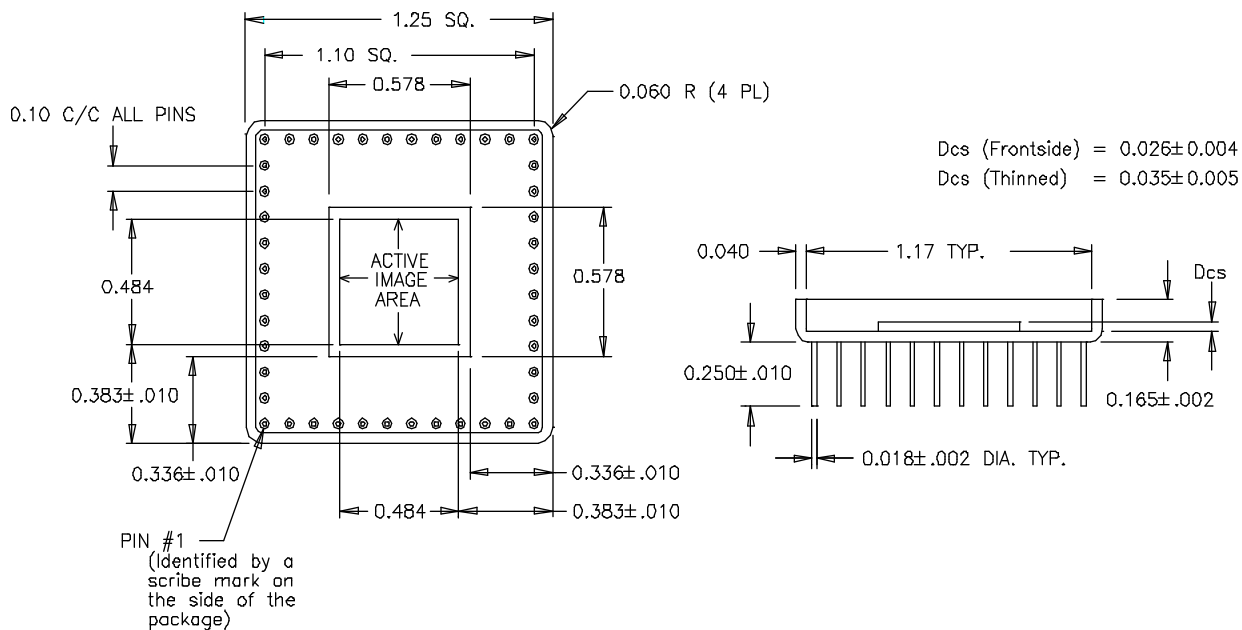


FIGURE 6 SI-502A package configuration

Quantum Efficiency vs. Wavelength (@ room temp)

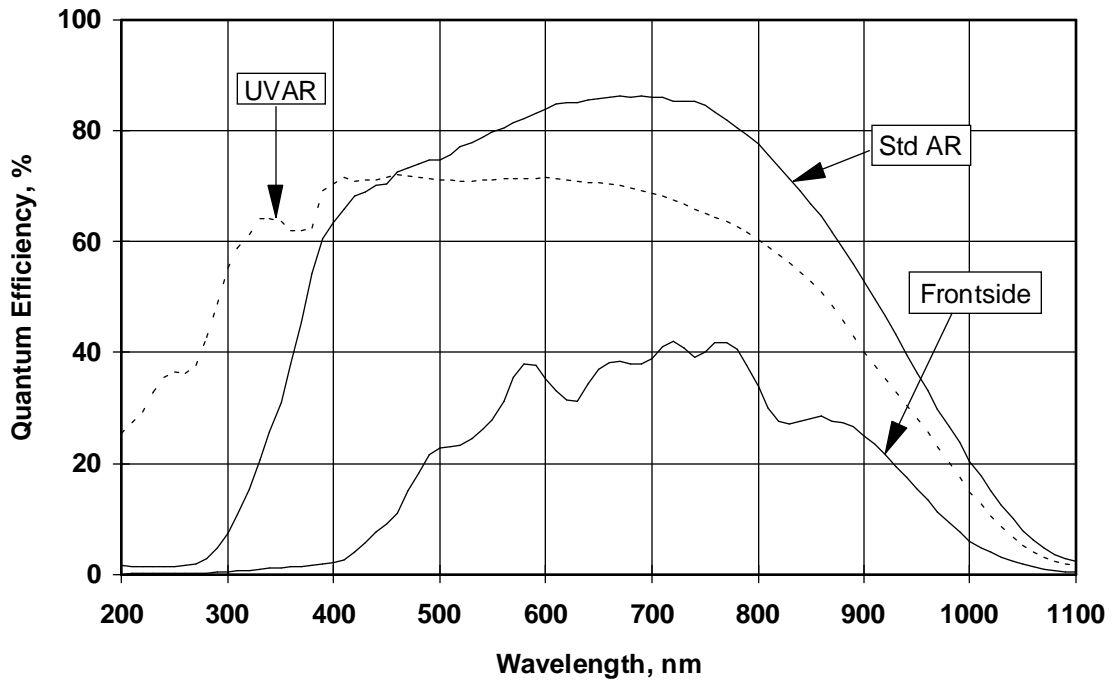


FIGURE 7 Typical QE curves

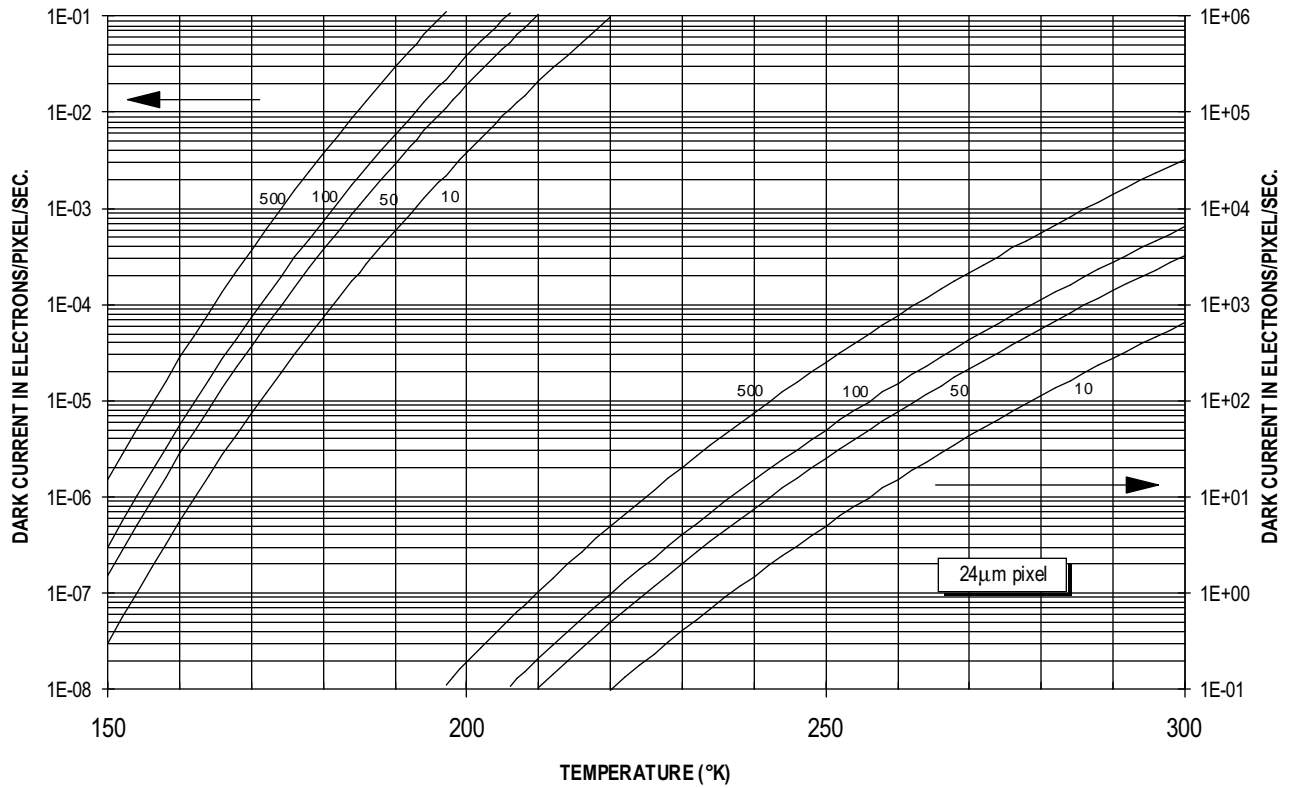


FIGURE 8 Effect of temperature on dark current. Parameter is $pAmp/cm^2$ at 293K



Product Precautions

Scientific Imaging Technologies, Inc. (SITe) realizes the use of charge-coupled devices (CCDs) for imaging is rapidly expanding into new applications. Awareness of the sensitivity of CCDs to electrostatic discharge (ESD) damage and the steps that can be implemented to prevent damage are very important to the end user.

With the exception of the back-illuminated SI424A, SITe imagers do not have built-in gate protection structures. Even with the protection structures, the imagers are very sensitive to ESD damage. It is imperative that proper precautions be taken whenever the imagers are handled.

The damage caused by ESD can be immediate and fatal (hard damage) resulting in a completely nonfunctional device. ESD damage can also be more subtle with no immediate device performance degradation. In this case, the result is a slow deterioration (soft damage) that may not be apparent until after extended operation.

There are three major areas where special procedures are required. We recommend that our customers use these procedures to minimize the risk of ESD damage.

1. Work areas specifically designed to minimize ESD.
2. Personnel requirements for ESD damage protection.
3. Use special ESD protected handling and shipping containers. SITe has developed a custom shipping container which grounds all the CCD pins together and allows clean and safe handling for incoming inspection and storage.

For more specific information on minimizing ESD damage, refer to SITe's technical briefing called "Recommended ESD Handling Procedures For CCD Imagers."

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Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include such areas as biomedical imaging, manufacturing quality control, environmental monitoring, and nondestructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications including NASA programs, satellite platforms, and other research projects. Device formats are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974.

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